EE437: Integrated Systems Capstone
EE536: Design of Analog Integrated Circuits and Systems
(Joint Offering)

Spring Quarter 2021

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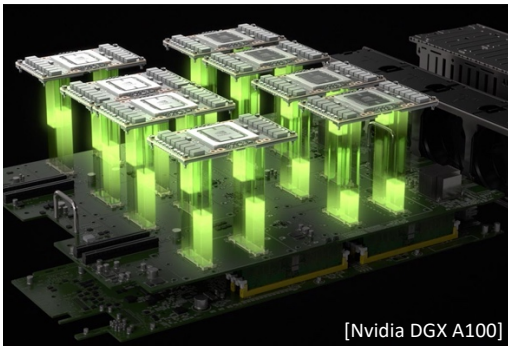
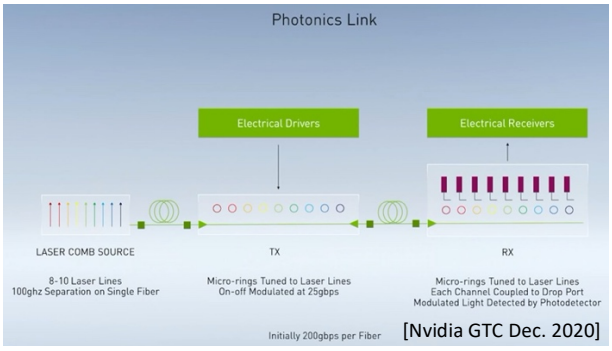
Ever-increasing size and complexity of artificial intelligence (AI) and machine learning (ML) models and datasets created a vital need for low-latency multi-Tb/s inter/intra-rack optical communications as well as low-latency chip-to-chip interconnects. For example, latest Nvidia DGX A100 systems consist of eight GPUs, each requiring 4.8Tb/s aggregate off-chip bandwidth. Although state-of-the-art inter-chip interconnects are realized via electrical wirelines, they cannot meet the stringent speed, energy-efficiency, and bandwidth density requirements of emerging AI supercomputers and hyper-scale datacenters. Silicon photonic transceivers have shown a great promise to address this challenge by ultimately 3D integrating optical transceivers with high performance processors in a same package. This fact is evident by recent announcements from Nvidia and Broadcom on co-packaging silicon photonics with next-generation GPUs and Network Switches. These co-packaged optics should provide multi-Tb/s aggregate data-rates at sub-pJ/b energy-efficiency. In this course, you will learn about the latest transceiver architectures and implementations, challenges of CMOS circuit design for +100Gb/s data-rates and multi-level modulations.


[Nvidia DGX A100]



[Nvidia GTC Dec. 2020]

Lecture Topics:

- Basics of wireline interconnects: transceiver architectures, equalization techniques (CTLE, DFE, FFE), high-speed DAC and TIA/Sense-amp design, …
- State-of-the-art of optical transceivers and design methodologies for +100Gb/s data-rates
- Trade-offs in electronic-photonic co-optimization
- Designing and simulating a full optical transceiver in Cadence

Prerequisites:

EE332 (*EE433 and EE473 requirements are waived for Spring 2021)

Students are expected to know circuits at the EE332 level or beyond, and previously used Cadence to design and simulate circuits.
If you are interested in taking this course and have any questions, please email the instructor!